

**324454 (25)**

**BE (4<sup>th</sup> Semester)**

**Examination, Nov.-Dec., 2021**

**Branch : Elect.**

**DIGITAL ELECTRONICS & LOGIC  
DESIGN (NEW)**

*Time Allowed : Three Hours*

*Maximum Marks : 80*

*Minimum Pass Marks : 28*

**Note :** Attempt all questions. Part (a) of all question is compulsory. Attempt any two part from (b), (c) and (d).

- Q. 1.** (a) What are the application of Gray codes. 2
- (b) Do the following : 7
- (i) Convert  $(1010000)_{\text{gray code}}$  to its equivalent decimal number.

(2)

(ii) Divide  $(11011.10)_2$  by  $(101)_2$ .

(iii) Convert gray code 10011011 into binary.

(iv) Represent CSVTU in EBCDIC code.

(c) Explain and state principle of duality. 7

(d) What is Hamming Code. Explain a typical data transmission system with error detection. 7

**Q. 2.** (a) Why and which code is used for labelling the cell of K-map. 2

(b) What do you mean by min-terms and max terms. Explain with suitable example. 7

(c) Find reduced SOP form for following equation: 7

$$F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 5, 8, 14)$$

(3)

(d) Simplify minimize Boolean function in SOP.

using don't care condition : 7

$$f = \overline{B}\overline{C}\overline{D} + B\overline{C}\overline{D} + ABC\overline{D}$$

$$d = \overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D}$$

Q. 3. (a) Define combinational circuits. 2

(b) Implement a full subtractor using two half subtractor and OR gate. 7

(c) Explain parallel binary adder. 7

(d) Explain 8421 BCD adder circuit using IC 7483. 7

Q. 4. (a) Write difference between Synchronous & Asynchronous counter. 2

(b) What is race around condition for J-K Flip-flop. How it can be eliminated. 7

(4)

- (c) Design a Synchronous Decade Counter. 7
- (d) Draw the logic diagram of 4 bit Johnson ring counter. 7
- Q. 5. (a) What is tristate logic. 2
- (b) Give comparison among various logic families. 7
- (c) Design NAND, NOR gate using CMOS logic. 7
- (d) Explain the following term : 7
- (i) Propagation Delay
- (ii) Speed power product.
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